CREATION OF ALGORITHMS FOR CALCULATING COEFFICIENTS IN PARTIAL POLYNOMIAL BASES OF KHAAR

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ABSTRACT

In this article, parallel algorithms have been developed for digital signal processing on piecewise-polynomial basis of Haar which is based on Analog Devices' Blackfin ADSP-BF561 dual-core processors. Based on these algorithms, developing of dual-core parallel computing program on VisualDSP++ has been considered. Functional descriptions of the Blackfin ADSPBF561 dual-core processor architecture are given. The architecture and components of the processor core have been described.

Keywords: Blackfin processors family; ADSPBF561 processors; dual-core processors; processor architecture; digital signal processing; Haar basis function;

INTRODUCTION

Today, digital signal processing technology is commonly being used in practice and with the help of it, it is increasing work efficiency. Digital signal processors and digital signal processing methods are used to solve problems in communications, radio engineering, electronics, acoustics, and seismology, television and control systems. Digital signal processors are manufactured by three major companies: Analog Devices, Freescale and Texas Instruments. These companies are also developing a multi-core signal processor designed to increase data processing capacity and processing speed. Blackfin ADSP-BF561 processors are a symmetrical dual-core special processor. The ADSPBF561 processor uses a hierarchical three-level memory model. The first level L1 memory operates at the clock frequency of the core, but the memory capacity is not very large. Each Blackfin core has its own 100 Kbytes of L1 memory and it includes:

- SRAM / cache 16 K bytes of command memory
- SRAM 16 K byte command memory
- SRAM / cache 32 K bytes of data memory
- SRAM 32 K bytes of data memory
- SRAM scratchpad 4 K bytes of RAM

Multi-Core Connections. The Single Application / Dual Core approach uses advanced linking tools to resolve interactions between cores and shared memory. Each kernel is defined by a PROCESSOR directive, and together is defined by two areas of memory (internal L2 memory and external memory) and one COMMON_MEMORY (shared memory) directive.

Both the PROCESSOR directive and the COMMON_MEMORY field can communicate with libraries as shown in Figure 2. Plibs libraries are represented directly according to PROCESSOR instructions. The objects of these libraries are private and are represented in the private memory of the A core or B core. Libraries specified as CLib are represented in the COMMON_MEMORY field. The objects of these libraries are stored in shared memory and can be accessed by both cores. If external data is linked using these libraries, this data is represented in the COMMON_MEMORY field and can be shared between core A and core B. Common code and data can be represented in the sml2 project in the L2 internal memory or in the sml3 project in the external memory.

Processor Core Architecture. Each core of the Blackfin ADSP-BF561 processor has two 16-bit multipliers, two 40-bit batteries, two 40- bit arithmetic logic devices (ALDs), four 8-bit video ALDs, and one 40-bit drive. Computing units process 8-, 16, or 32-bit data from a registry file.

There are three different types of software design for dual-core Blackfin processors on the VisualDSP++ platform: - Single-core applications. In this project, only core A is used, while core B is not active. - One application per core. In this project, each bar core is seen as a separate processor. VisualDSP++ creates a .dxe file for a specific core in the project. Resource sharing is managed by programmers.

CONCLUSION

As can be seen from Table 1, a dual-core processor consumes 1.9 to 1.98 times less time than a single-core processor. Hence, the parallelization of calculations using multi-core processors allows to reduce the time spent and increase the efficiency compared to single-core computing. The main advantage of developing parallel applications for dual-core processors on the VsiualDSP++ platform is that, it creates a separate subprogram for each core and shared memory. This allows different calculations to be performed in parallel at the same time in each core. The two cores can use the common data and functions represented in the L2 shared memory project in parallel at the same time.

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